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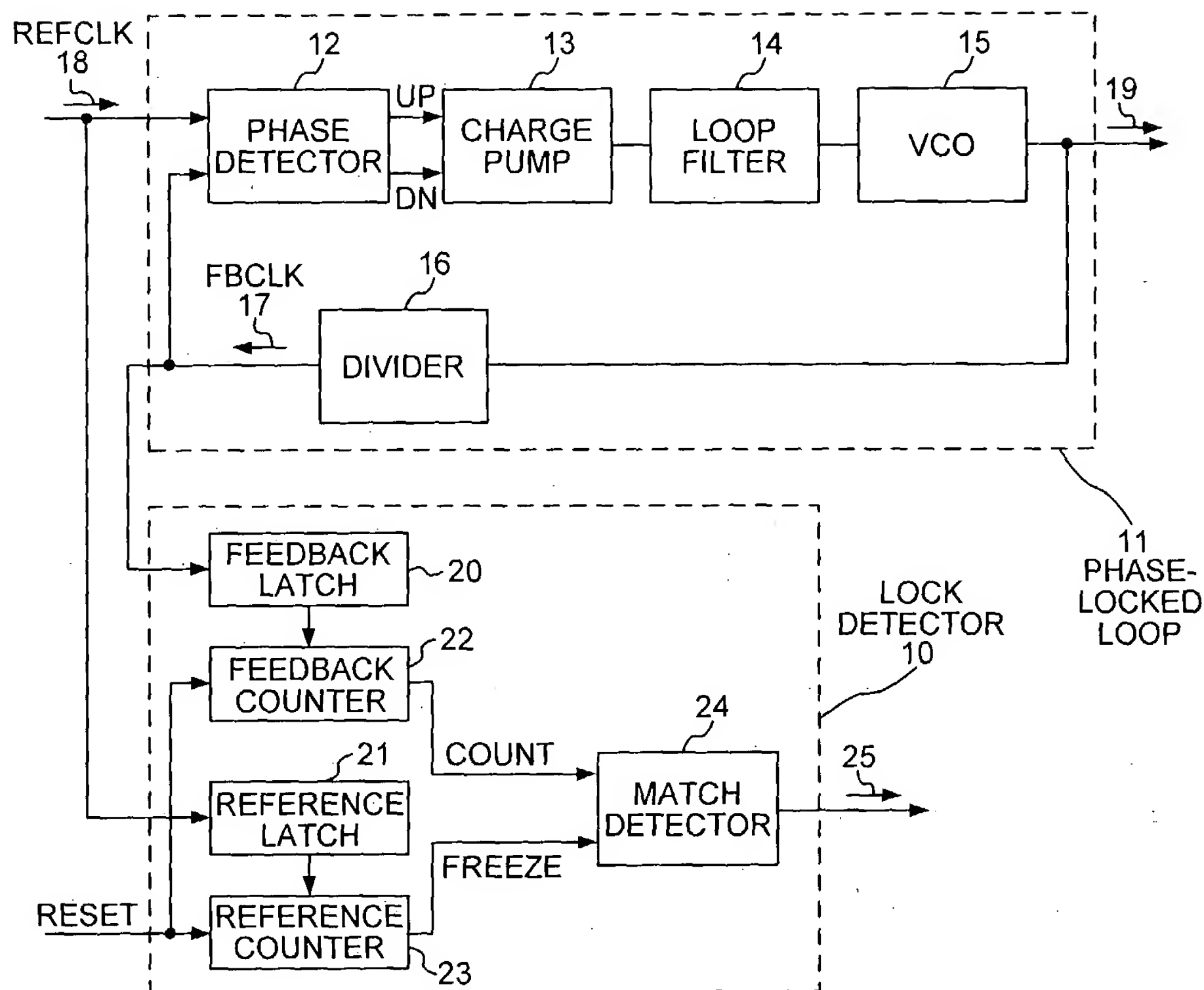


FIG. 1
(PRIOR ART)

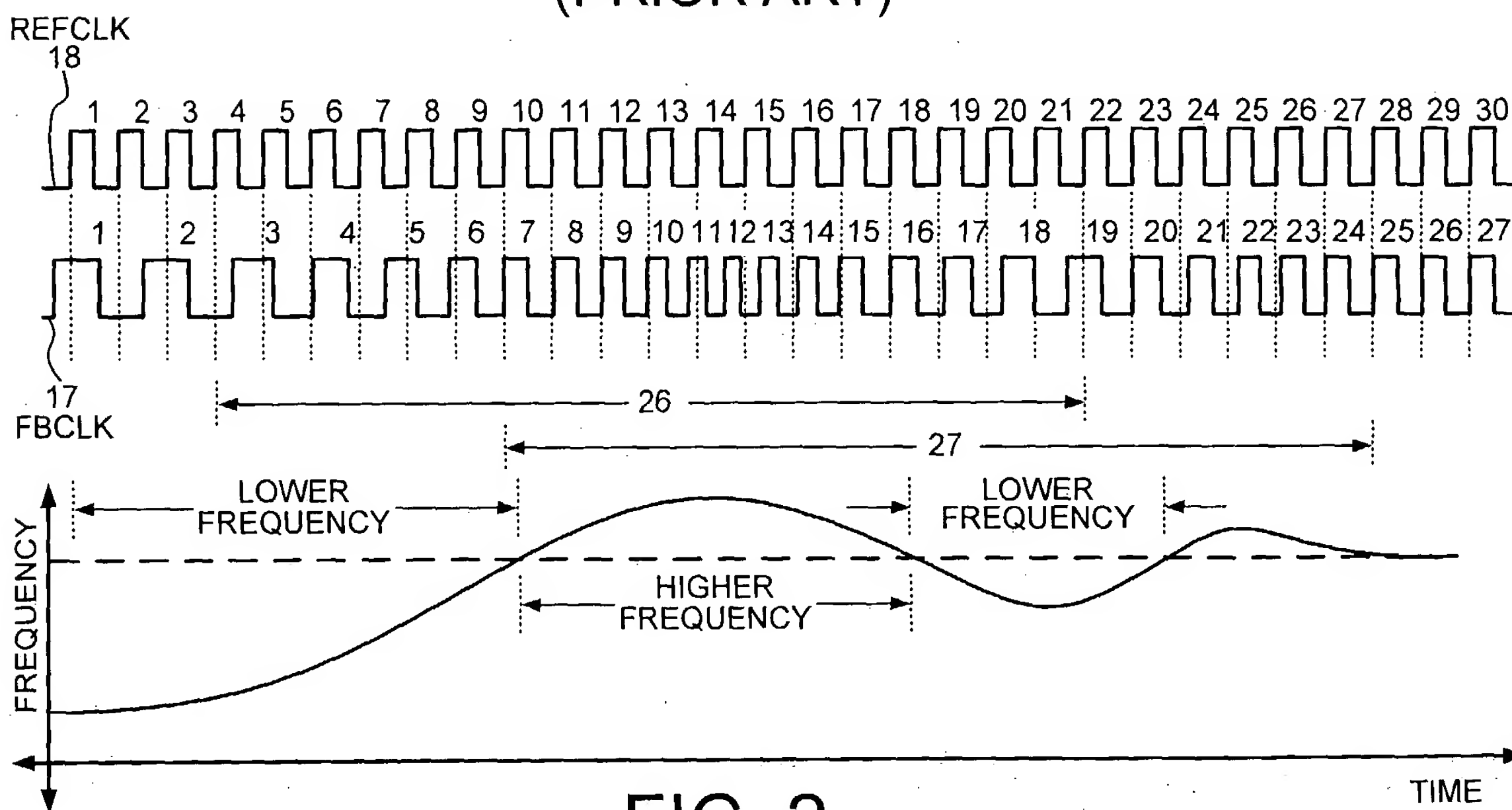


FIG. 2
(PRIOR ART)

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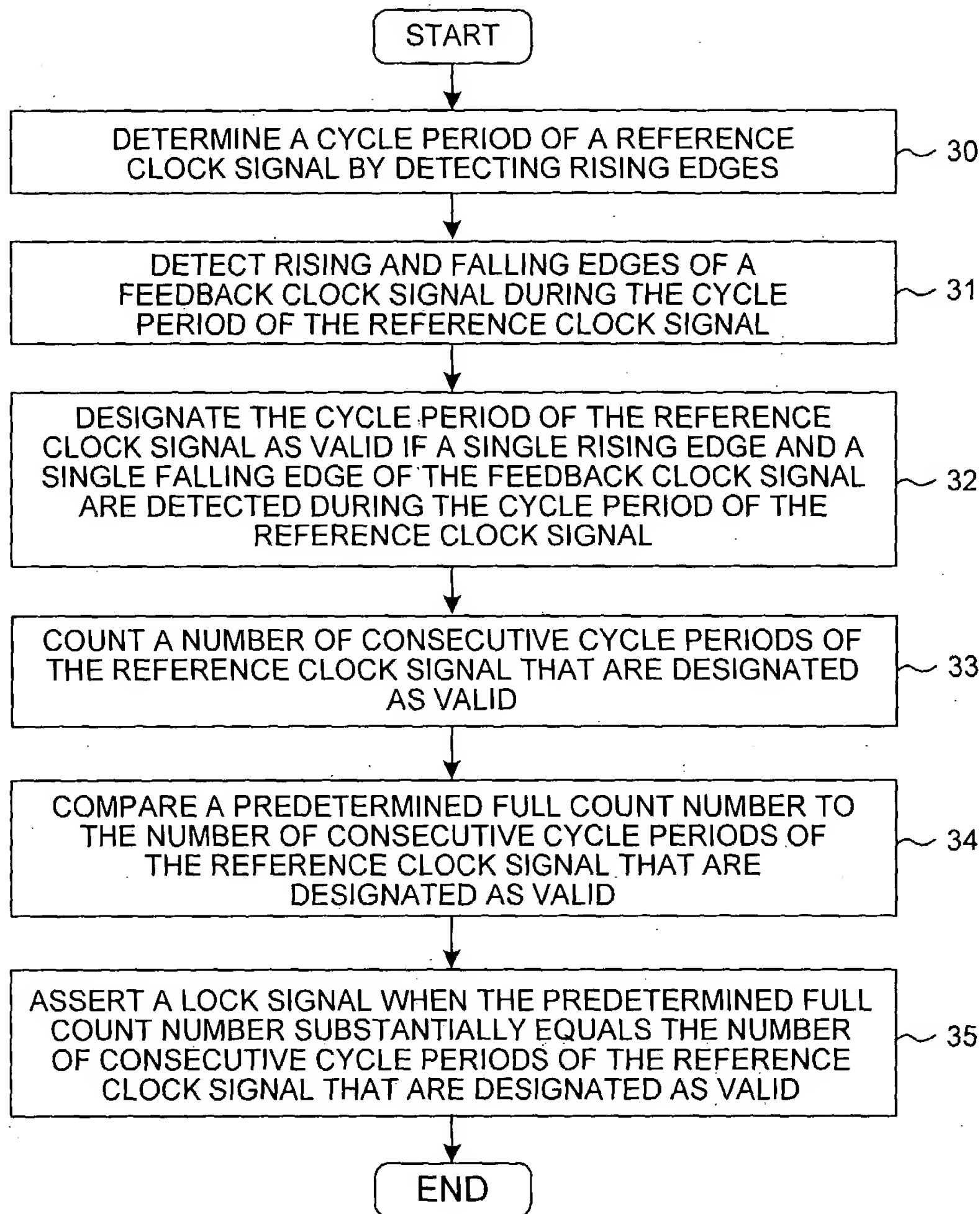


FIG. 3

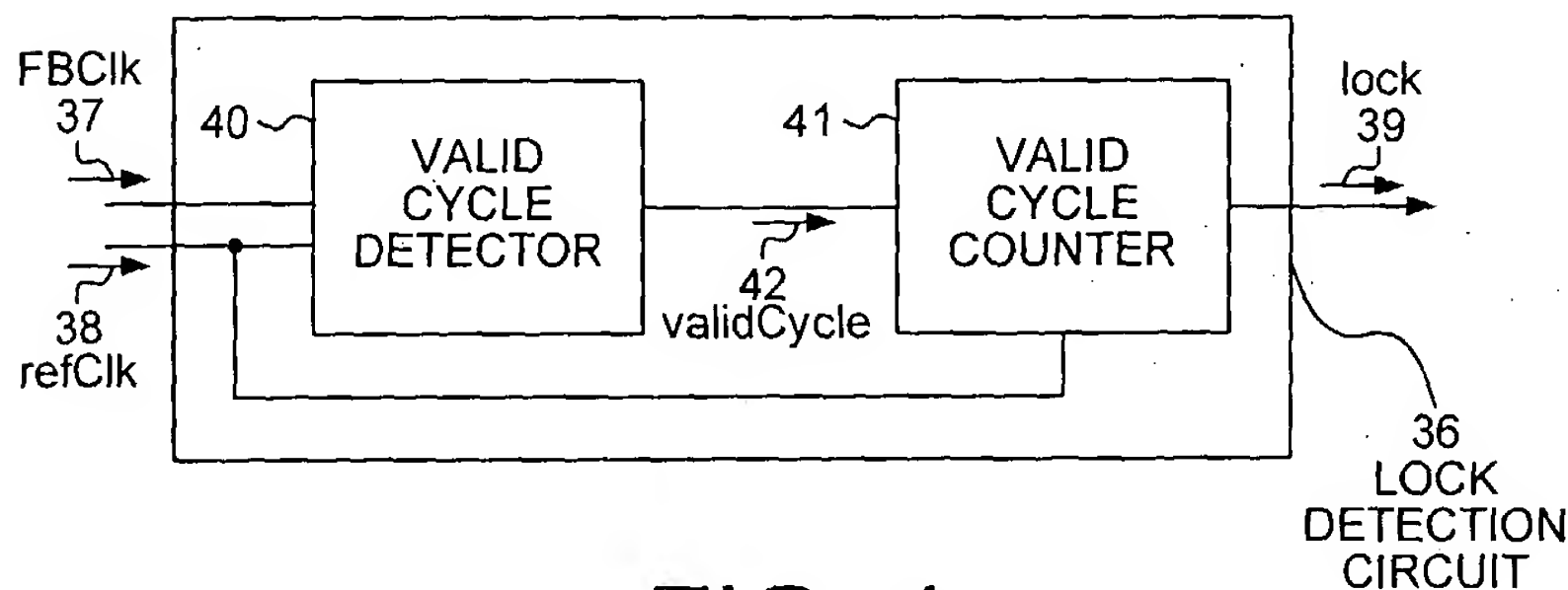


FIG. 4

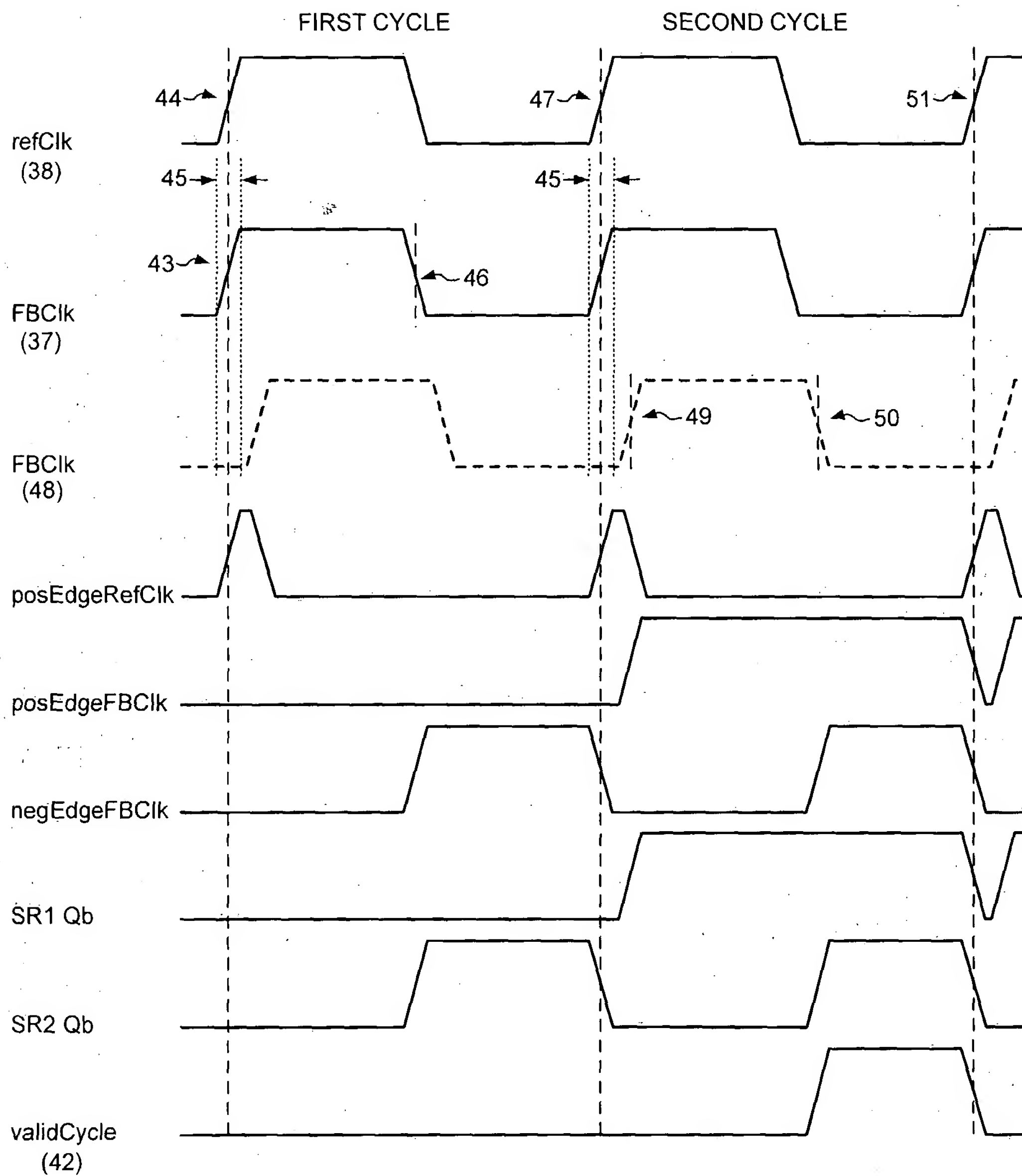


FIG. 5

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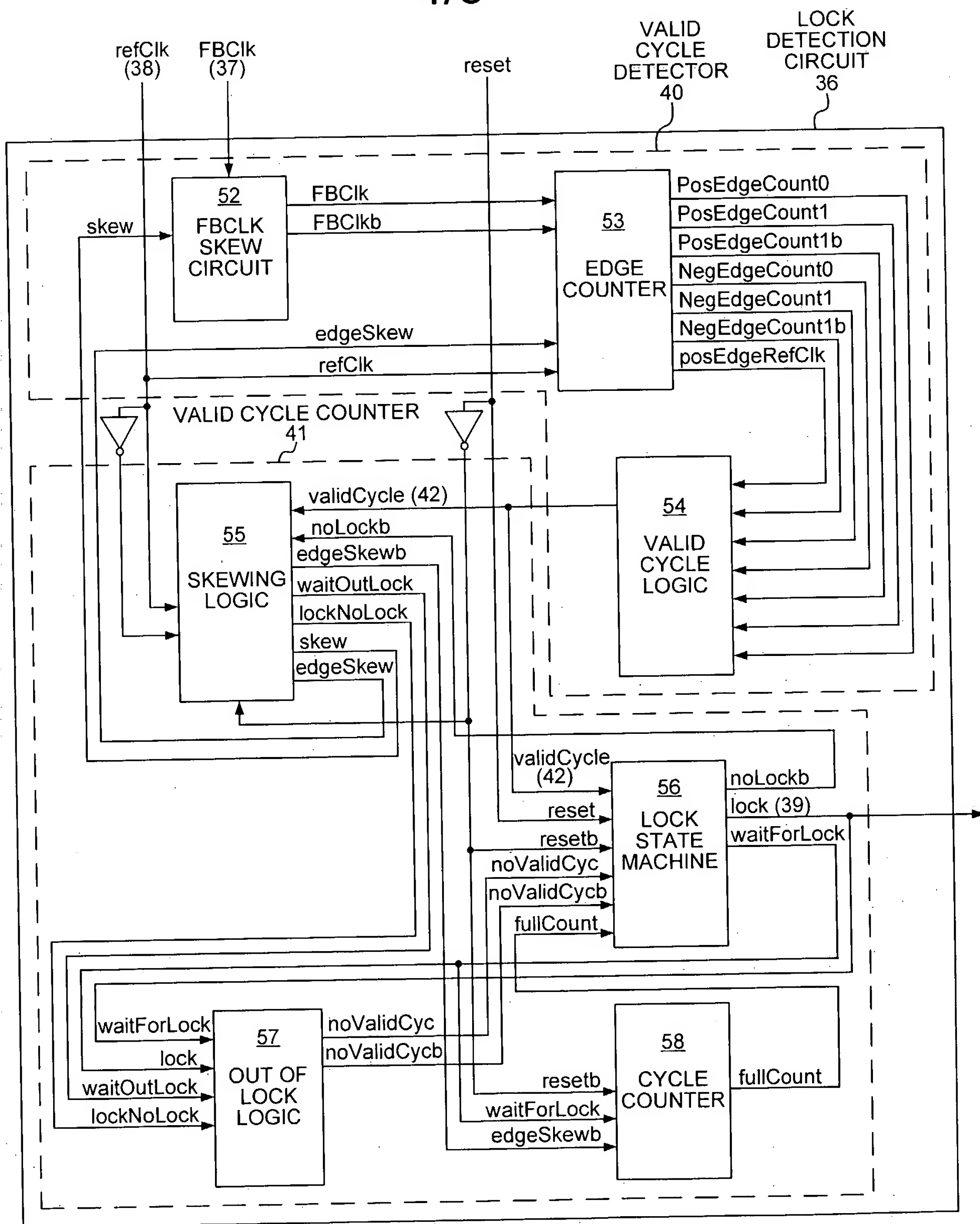


FIG. 6

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STATES OF VALID
CYCLE COUNTER

CURRENT STATE	INPUT SIGNALS	waitOutLock SIGNAL	NEXT STATE	OUTPUT VALUES
0 0 1	0 0 0	X	0 0 1	0 0 1
0 0 1	0 0 1	X	0 0 1	0 0 1
0 0 1	0 1 0	X	0 1 0	0 0 1
0 0 1	0 1 1	X	0 1 0	0 0 1
0 0 1	1 0 0	X	0 0 1	0 0 1
0 0 1	1 0 1	X	0 0 1	0 0 1
0 0 1	1 1 0	X	0 1 0	0 0 1
0 0 1	1 1 1	X	0 1 0	0 0 1
0 1 0	0 0 0	X	0 1 0	0 1 0
0 1 0	0 0 1	X	NOT POSSIBLE	0 1 0
0 1 0	0 1 0	X	NOT POSSIBLE	0 1 0
0 1 0	0 1 1	X	NOT POSSIBLE	0 1 0
0 1 0	1 0 0	X	1 0 0	0 1 0
0 1 0	1 0 1	X	NOT POSSIBLE	0 1 0
0 1 0	1 1 0	X	NOT POSSIBLE	0 1 0
0 1 0	1 1 1	X	NOT POSSIBLE	0 1 0
1 0 0	0 0 0	0	1 0 0	1 0 0
1 0 0	0 0 1	0	1 0 0	1 0 0
1 0 0	0 1 0	0	NOT POSSIBLE	1 0 0
1 0 0	0 1 1	0	NOT POSSIBLE	1 0 0
1 0 0	1 0 0	0	1 0 0	1 0 0
1 0 0	1 0 1	0	0 0 1	1 0 0
1 0 0	1 1 0	0	NOT POSSIBLE	1 0 0
1 0 0	1 1 1	0	NOT POSSIBLE	1 0 0
1 0 0	0 0 0	1	0 1 0	1 0 0
1 0 0	0 0 1	1	0 1 0	1 0 0
1 0 0	0 1 0	1	NOT POSSIBLE	1 0 0
1 0 0	0 1 1	1	NOT POSSIBLE	1 0 0
1 0 0	1 0 0	1	1 0 0	1 0 0
1 0 0	1 0 1	1	0 0 1	1 0 0
1 0 0	1 1 0	1	NOT POSSIBLE	1 0 0
1 0 0	1 1 1	1	NOT POSSIBLE	1 0 0

waitForLock
noLock
lock

validCycle (42)
noValidCyc
fullCount

waitForLock
noLock
lock

waitForLock
noLock
lock

FIG. 7

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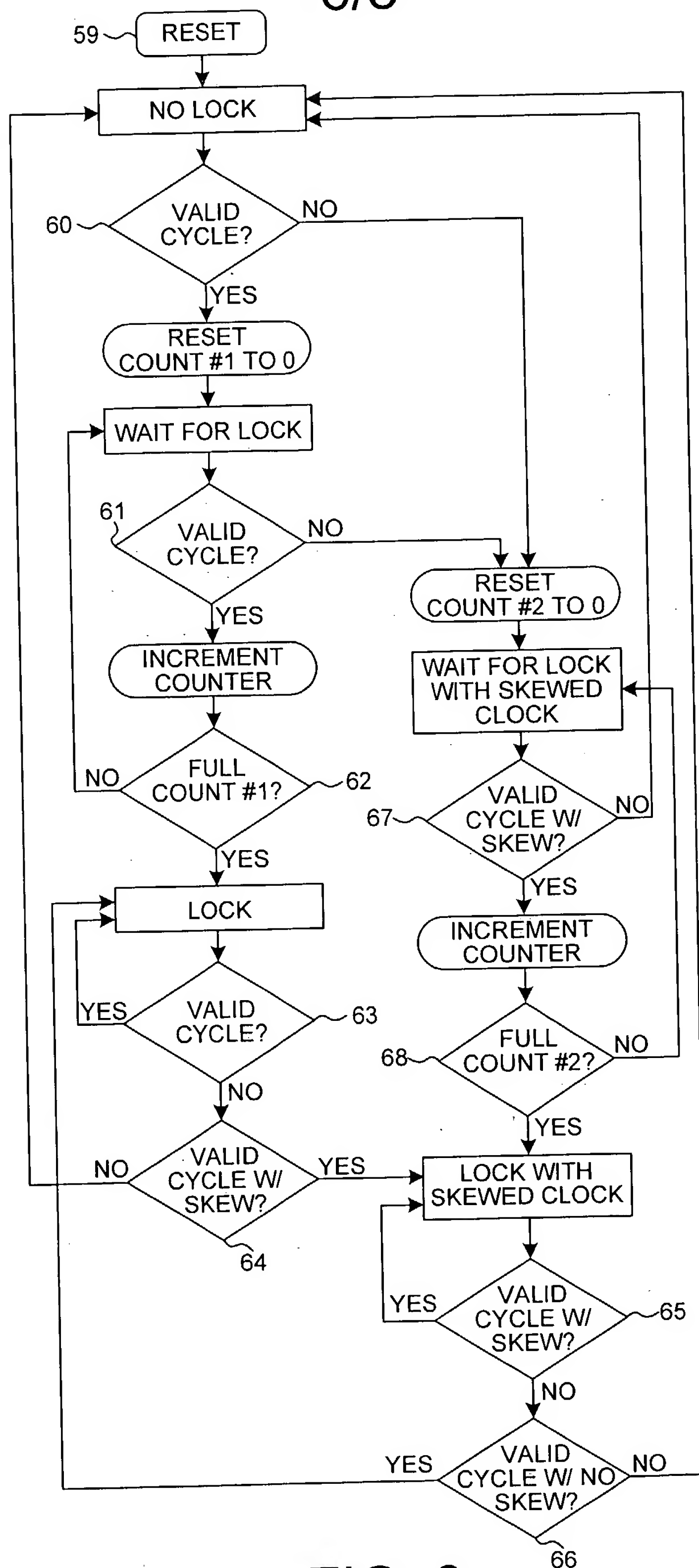
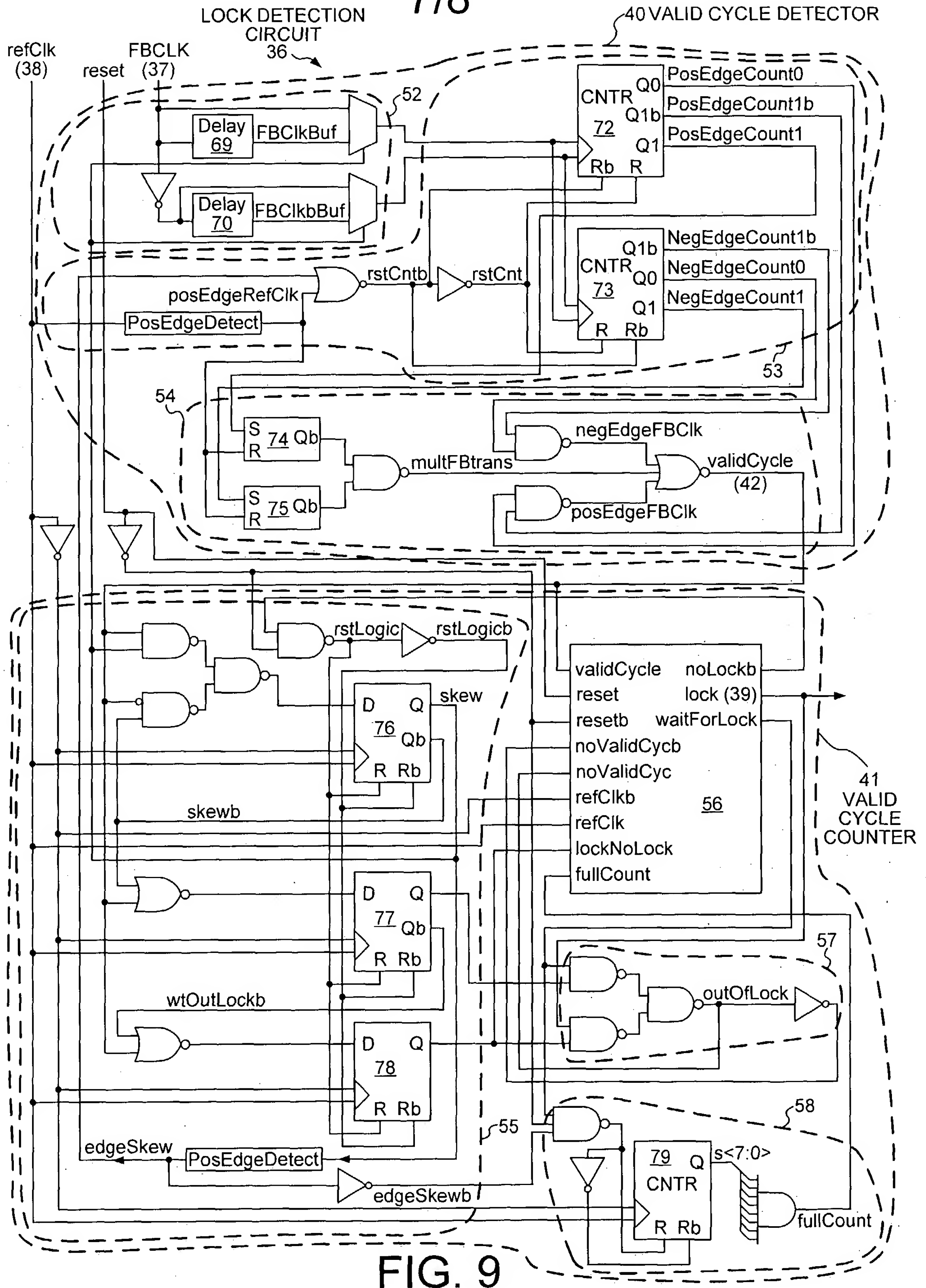


FIG. 8



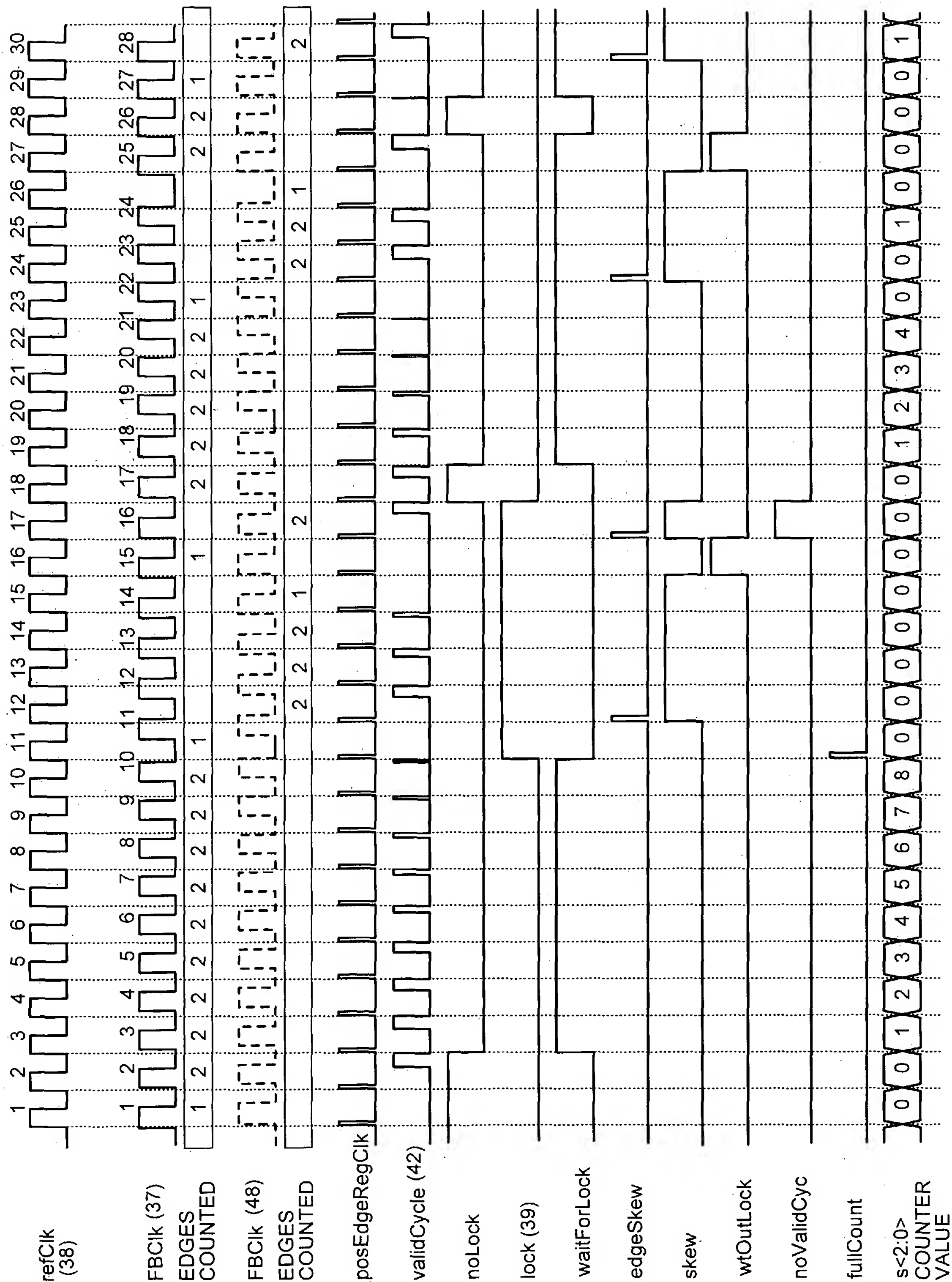


FIG. 10